WHAT IS CLAIMED IS:

1. An integrated-circuit apparatus comprising a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals, wherein

the circuit blocks respectively output an initialization completion signal for communicating completion of initialization after they are initialized, and

the CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with initialization completion signals output from the circuit blocks.

2. The integrated-circuit apparatus according to claim 1, wherein

the circuit blocks of the integrated-circuit apparatus are initialized to output initialization completion signals, and

a logic circuit for inputting the initialization completion signals output from the circuit blocks to logic-operate the signals, and outputting the logic-operation results to the CPU is further included.

3. The integrated-circuit apparatus according to claim 1, wherein

when all of the circuit blocks are initialized, the CPU outputs the enable signal to all the circuit

blocks.

4. The integrated-circuit apparatus according to claim 2, wherein

when all of the circuit blocks are initialized, the CPU outputs the enable signal to all the circuit blocks.

5. The integrated-circuit apparatus according to claim 1, wherein

if there is any circuit block that is not initialized yet, the CPU initializes the circuit block by using the enable signal.

6. The integrated-circuit apparatus according to claim 2, wherein

if there is any circuit block that is not initialized yet, the CPU initializes the circuit block by using the enable signal.

7. The integrated-circuit apparatus according to any one of claims 1 to 6, wherein

the circuit blocks output the initialization completion signals when a predetermined period passes after the reset signal is input.

8. The integrated-circuit apparatus according to

any one of claims 1 to 6, wherein

the integrated-circuit apparatus is constituted of one chip.

9. The integrated-circuit apparatus according to claim 7, wherein

the integrated-circuit apparatus is constituted of one chip.

10. The integrated-circuit apparatus according to any one of claims 1 to 6, wherein

the integrated-circuit apparatus is used for a printer.

11. The integrated-circuit apparatus according to claim 7, wherein

the integrated-circuit apparatus is used for a printer.

12. The integrated-circuit apparatus according to claim 8, wherein

the integrated-circuit apparatus is used for a printer.

13. The integrated-circuit apparatus according to claim 9, wherein

the integrated-circuit apparatus is used for a

printer.

14. An ink-jet recording apparatus comprising an integrated-circuit apparatus for controlling the recording using a recording head, wherein

the integrated-circuit apparatus has a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals,

the circuit blocks respectively output an initialization completion signal for communicating completion of initialization after they are initialized, and

the CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with initialization completion signals output from the circuit blocks.

15. The ink-jet recording apparatus according to claim 14, wherein

the recording head has a control circuit and the circuit blocks respectively output a signal for initializing the control circuit.

16. The ink-jet recording apparatus according to claim 14, wherein

the ink-jet recording apparatus has a driving circuit for performing the above recording and the

circuit blocks respectively output a signal for initializing the driving circuit.

17. A control method of an integrated-circuit apparatus having a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals, comprising the steps of:

initializing the circuit blocks and outputting an initialization completion signal for communicating completion of initialization; and

outputting an enable signal for permitting operations of the circuit blocks in accordance with the signal output in the outputting step.